

TDES: Asynchronous DES IP

Version 2.3 - Nov 201

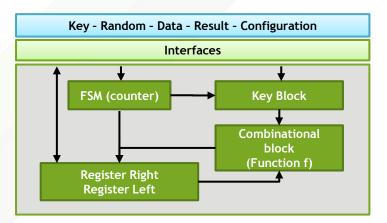
Tiempo clockless cryptoprocessor core - DES - is able to execute the standard encryption and decryption algorithms DES, DES-1, 3DES and 3DES-1. This IP is designed in Tiempo fully asynchronous and delay insensitive technology that allows ultralow power consumption, ultralow noise, ultra-low EMI, as well as robustness against attacks by power analysis & fault injection.

Applications

Targeted applications are chips for smart cards (with or without contact), RFID tags, sensor networks, systems embedding NFC technology and other secured applications



TDES Block Diagram



Key benefits

- Ultra low power consumption: low energy, low current peaks
- Ultra low electromagnetic emission (EMI/EMC)
- High speed under low/variable power (independently from system clock)
- High robustness against any PVT (process, voltage, temperature) variation
- High robustness against attacks by power analysis and fault injections (for secured applications)

Key features

- Executes standard encryption and decryption algorithms DES, DES⁻¹, 3DES and 3DES⁻¹
 - Data: 64 bits
 - Key: 56 or 112 bits
 - Triple DES modes supported with two or three keys
 - ECB and CBC modes supported
- Fully asynchronous (no clock) and delay insensitive (correctness of encryption / decryption is guaranteed regardless of any actual delay in internal gates and wires)
- Available as Verilog netlist ready for P&R (silicon-proven netlist) or as a GDSII hard-IP block (verified layout description)¹
- Option: IP secured against attacks by power analysis and fault injection

¹ Please contact Tiempo for available libraries and technologies

Silicon Proven

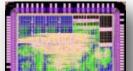
Designed and processed on TSMC CMOS 130 nm LP technology.

Characteristics

Figures below are electrical measurements made on Tiempo prototype chip TESIC fabricated on a TSCM130LP 1.5V process. Figures are valid for the *secured* version of the IP.

These figures illustrate one instance of the IP and can be tuned to our customer needs (reduced power consumption or increased performance).

Supply voltage	1.0V	1.5V
Encryption speed (µs)	3.17	1.31
Average current (mA)	0.31	1.07
Energy (nJ)	1.04	2.09



Tiempo TESIC chip



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